Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. No claims have been amended. Claims 11-15 have been canceled without prejudice.

Listing of Claims:

1. (Previously presented) A method, comprising:

manufacturing a processor having a flexible architecture to service a multiple processor platform as well as a different application platform, wherein the processor contains

a plurality of N-bit registers, wherein N-bit is any number,

an XN-bit register, wherein X is a whole number greater than one and acts as a multiplier on the value of N,

a multiplexer connected to each of the N-bit registers and the XN-bit register, and

an arbiter connected to the mulitplexer to direct the multiplexer to route signals from the N-bit registers or a signal from the XN-bit register depending upon the platform to be serviced.

2. (Original) The method of claim 1, further comprising:

manufacturing the processor to communicate with a device through a point to point bus.

3. (Previously presented) The method of claim 1, further comprising:

manufacturing the arbiter to alter one or more signal pathways that a signal may travel within the processor, the arbiter can alter the signal pathways without physically changing the flexible architecture inside the processor.

4. (Previously presented) An apparatus, comprising:

an arbiter linked to a first processor having a flexible architecture with a first port and a second port, wherein the first processor contains a multiplexer, a first bit register connected in a signal path of the first port and a second bit register connected in a signal path of the second port;

a point to point bus; and

a device, the first port connected to the device through the point to point bus, wherein the arbiter directs the multiplexer whether to route signals from the first bit register as well as from the second bit register.

5. (Original) The apparatus of claim 4, wherein the arbiter is internal to the first processor.

6. (Original) The apparatus of claim 4, wherein the arbiter is external to the first processor.

7. (Original) The apparatus of claim 4, wherein the arbiter comprises a component to change a number of ports linked between the first processor and the device without changing the flexible architecture within the processor.

8. (Original) The apparatus of claim 4, wherein the device is selected from the group consisting of an input-output component, a bridge, a chipset, a memory, or a second processor.

9. (Original) The apparatus of claim 4, wherein the processor comprises:

a protocol layer;

an information transfer layer to electronically transfer information on a physical medium between the protocol layer and the device; and

a buffer layer to buffer an electronic transfer of information between the protocol layer and the information transfer layer.

10. (Original) The apparatus of claim 4, wherein the arbiter comprises a first component and a second component, the first component to determine a bandwidth between the device and the processor, the second component to provide a control signal to one or more signal pathway switching devices, the control signal to be based upon the bandwidth determination of the first component.